

REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claims 1-13 stand rejected as allegedly being anticipated by Dresselhouse et al. (US 6,060,656) (hereinafter "Dresselhouse").

Claims 14-24 were acknowledged by the Examiner in the Office Action as comprising non-elected subject matter. These claims are thus withdrawn from consideration.

With respect to Claims 1-13, applicants respectfully disagree.

As a preliminary matter, applicants take this opportunity to amend Claim 1 to specifically and more accurately set forth the strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) transistor device having gate stress engineering with SiGe and/or Si:C, comprising:

a substrate of either bulk silicon (Si) or silicon on insulator (SOI), and a gate dielectric layer over the substrate;

a stacked gate structure of SiGe and/or Si:C to produce stresses by the structures of SSi(strained Si)/SiGe or SSi/Si:C in the stacked gate structure and having a first stressed film layer of large grain size Si or SiGe formed on top the gate dielectric layer, a second stressed film layer of strained SiGe or strained Si:C formed on top the first stressed film layer, and a semiconductor or conductor layer formed over the second stressed film layer.

The Examiner's attention is respectfully directed to the amendments made to Claim 1 which clarify the structure in greater detail. Particularly, amendments have been made to Claim 1 to set forth that the MOS (metal oxide semiconductor) device is a transistor device,

and further, that the stacked gate structure includes: the gate dielectric, and, the first stressed film layer of large grain size Si or SiGe formed on top the gate dielectric layer, and second stressed film layer of strained SiGe or strained Si:C formed on top the first stressed film layer, and, a semiconductor or conductor layer formed over the second stressed film layer.

Respectfully, Dresselhaus is not even close to the structure of the present invention as claimed as the present claimed structure is directed to a MOSFET transistor device and Dresselhaus' device is directed to a thermoelectric device having a superlattice structure of alternating layers of Si and SiGe having a thermoelectric figure of merit.

To the contrary, the MOSFET transistor device of the present invention as set forth in amended Claim 1 includes a gate oxide layer that separates the gate (Si/SiGe layers) from substrate (SOI or bulk Si). Dresselhaus' device does not have a stacked gate structure including a gate oxide that separates a Si/SiGe super lattice layer from substrate as now required by the Claim 1 (now amended). As such, Dresselhaus cannot be said to be anticipate Claim 1 of the present invention.

An additional amendment is being submitted to remove the specified limiting recitation "such as p(poly)-Si over" language present in Claim 1 directed to the type of top layer material in the stacked gate structure.

Respectfully, as the thermoelectric device of Dresselhaus is quite different from the present invention as claimed in amended Claim 1, the Examiner is respectfully requested to withdraw the rejection of independent Claim 1 and all pending claims dependent thereon under 35 U.S.C. 102(b).

In view of the foregoing, this application is now believed to be in condition for

allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,


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